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# SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

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Inventor: MATSUMOTO MICHIICHI; FUJII MINORU; YABU TOSHIKI
Applicant: MATSUSHITA ELECTRIC IND CO LTD
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Abstract of JP9074199

PROBLEM TO BE SOLVED: To provide a semiconductor device having silicide structure wherein an FET having a low resistance value corresponding to a fine pattern is arranged. SOLUTION: A polysilicon electrode 4a is formed, via a gate oxide film 3, on a polysilicon substrate 1 in an active region surrounded by element isolation. A polysilicon wiring 4b is formed on the element isolation. A source.drain region 8 is formed on both sides of the polysilicon electrode 4a. On both sides of polysilicon, films constituting the electrode 4a and the wiring 4b, side walls 7a, 7b whose heights are at most 4/5 of the height of the polysilicon films are formed. Silicide layers 9a, 9b are formed which are in contact with the upper surfaces of the polysilicon films and the parts above the side walls on both side surfaces. A silicide layer 9c which is in contact with the source drain region 8 is formed. Since the sectional areas of the silicide layers 9a, 9b are enlarged, low resistance can be maintained even when the size of the polysilicon films is made fine.